REMARKS/ARGUMENTS

Claims 1, 2, 4-11, 13-25, 27-34 and 36-47 stand rejected in the outstanding Official Action. Claims 1, 24 and 47 have been amended and therefore claims 1, 2, 4-11, 13-25, 27-34 and 36-47 remain in this application.

The Examiner's confirmation of PTO acceptance of the previously filed formal drawings is very much appreciated. Similarly, the Examiner's acknowledgment of Applicants' claim for foreign priority and receipt of the certified copies of the priority documents is very much appreciated.

In section 5 on page 5 of the Official Action, the Examiner indicates that the previous obviousness rejections of claims 8-10, 14-19, 31-33 and 37-42 over the Christie and Knight references is withdrawn. Inasmuch as there are no other obviousness-type rejections (other than the obviousness-type double patenting rejection which is cured by the attached terminal disclaimer), these claims are understood to contain allowable subject matter and to be allowable if rewritten in independent form. This notification by the Examiner is very much appreciated.

In sections 7, 8, 9 and 10 of the Official Action, the pending claims are rejected under the grounds of obviousness-type double patenting over copending Application Serial No. 10/714,518 and issued U.S. Patents 7,117,284, 7,305,712 and 7,124,274. Applicants' undersigned representative encloses herewith a Terminal Disclaimer agreeing to maintain these patents and applications as commonly assigned. It is noted that all of these patents and patent applications were filed in the United States on November 17, 2003, and, but for variations in the term extensions due to PTO delays, will all expire together

Therefore, in view of the submitted Terminal Disclaimer, the obviousness-type double patenting rejections set forth in sections 7-10 of the outstanding Official Action are obviated and any further objection or rejection thereto is respectfully traversed.

Claim 47 stands rejected under 35 USC §101 as being directed to non-statutory subject matter. Claim 47 has been amended to recite that the computer program product comprises "a computer readable storage medium." U.S. PTO patent practice has confirmed that where a computer program product is recited in the specification, the specification inherently discloses a "computer readable storage medium" upon which the computer program product is recorded. In accordance with this PTO policy decision, there can be no objection based on entry of "new matter" with respect to the amendment to claim 47. It is further noted that the amendment to claim 47 is similar to the existing approved claims in U.S. Patent 6,836,860 (claim 1) also directed to a computer program product. Accordingly, any further rejection or objection to claim 47 is respectfully traversed.

On page 9, section 12 of the Official Action, the Examiner rejects claims 1, 2, 4-7, 11, 13, 20-25, 27-30, 34, 36 and 43-47 under 35 USC §103 as unpatentable over Christie (U.. Patent 7,165,135) in view of Knight (U.S. Publication 2003/0126520). Furthermore, on page 13, section 13, claims 1 and 24 are rejected under 35 USC §103 as being unpatentable over Christie in view of Dahan (U.S. Patent 7,237,081).

While the outstanding Official Action provides generalities as to where claimed structures and claimed interrelationships between structures are disclosed in the three cited references, a detailed review of each of these references will show that none of them disclose

features of Applicants' independent claims 1 and 24 and therefore cannot disclose or render obvious any of the claims in the present application.

The Elements/method steps and interrelationships are set out in the independent claims. Applicants' original claims 1 and 24 recite "said one or more exception conditions have **respective programmable configurations associated therewith** that control triggering of either a non-secure exception handler . . . or a secure exception handler . . . ." None of the three cited references disclose this claimed feature. While the Examiner has not objected to the language of this positively recited interrelationship as indefinite, Applicants have amended claims 1 and 24 so that the clause reads "at least two of said one or more exception conditions have respective programmable configurations associated therewith." It is clear from the language of the claim that control triggering of either a non-secure exception handler or a secure exception handler requires at least two exception conditions and therefore this recognized interrelationship has been added to independent claims 1 and 24.

Additionally, to avoid any possibility that the Examiner or Board in the future will ignore the recited processor configuration of "said processor being operable to select said exception handler from among a plurality of possible exception handlers in dependence upon an exception vector value . . . ," Applicant has amended the language to read "said processor configured to select . . . ," which language is more in consistence with PTO claiming policies.

Therefore, as noted above, it is necessary for the Examiner in order to meet his burden of establishing a *prima facie* case of obviousness to show where or how claimed elements and claimed interrelationships between elements are disclosed in at least one of the combination of references. This detailed disclosure will clearly show that none of Christie, Knight and Dahan

disclose the "respective programmable configurations associated therewith" structure and interrelationship between structures that is specified in independent claims 1 and 24.

1. The Christie reference does not teach "respective programmable configurations associated therewith."

In the Official Action on page 10, lines 4-9, the Examiner cites various portions of the Christie reference as allegedly teaching the claimed "respective programmable configurations associated therewith." However, as will be seen, none of these sections actually describes any programmable configuration as required by independent claims 1 and 24.

The Examiner cites "Fig. 3" but Figure 3 shows the SEM (secure execution mode) processor. While it does show exception logic 170 which is responsive to interrupt signals SMI and INIT, it does not show any "programmable configurations" that are associated with the respective interrupt signals.

The citation to column 4, lines 29-67 in the Christie reference describes the normal execution and secure execution modes, but does not describe anything relating to "exception handling" as required by the claims.

Column 9, line 62 to column 10, line 67 describes the processing that occurs in Christie when an interrupt is encountered. The only interrupts described are the SMI and INIT interrupts. There is no disclosure of "programmable configurations" that are associated with "respective" interrupt types to control triggering either non-secure or secure exception handling as required by independent claims 1 and 24.

In lines 8 and 9 on page 10, the Examiner alleges that Christie discloses a "controller, or mode capable processor to control exception handling based on modes/domains." Even if true,

this statement does not demonstrate that Christie discloses the claimed "respective programmable configurations associated therewith."

Moreover, a controller that controls exception handling based on modes/domains is not the same structure as the claimed feature wherein each exception condition has "respective programmable configurations associated therewith" for controlling the triggering of either a non-secure exception handler or a secure exception handler.

How or why the Examiner believes any of the above cited Christie statements demonstrate that the Christie teaches the claimed "respective programmable configurations associated therewith" is simply not seen and clarification is respectfully requested.

It should also be understood that Christie's process for choosing an exception handler is shown in Figures 4 and 5. Figure 4 shows the processing for the SMI interrupt and Figure 5 shows the processing for the INIT interrupt. Neither of these processes uses programmable configurations. Thus, even if these Christie processes are the ones referenced by the Examiner, the decision of which handler to use (normal processing or the security exception) is determined based on the **current mode of the processor only**.

The current mode of the processor is not "programmable" nor is it associated with any particular exception condition and so cannot be considered a "programmable configuration" as described in the independent claims. Clearly, the Christie reference does not support the Examiner's obviousness rejection.

2. The Knight reference does not teach "respective programmable configurations associated therewith."

Turning to the Knight patent, it also fails to disclose the claimed "programmable configurations." On both the paragraph bridging pages 3 and 4 of the Official Action and on page 10 of the Official Action, the Examiner cites paragraph 0007 and 0015-0019 of the Knight reference as purportedly teaching the claimed programmable configurations. The Knight reference does not disclose any non-secure or secure modes/exception handlers, but even if it did, it would not disclose programmable configurations.

The Examiner alleges with reference to Knight that "each exceptions [sic] has corresponding operational modes" (Official Action page 4). The cited paragraph 0019 of the Knight reference states "ARM processors [include] several modes of operation. For example, 'user' and 'system' modes are used for normal program execution. In addition, each of the exceptions (IRQ, data abort, etc.) has a corresponding processor mode . . . ." However, nowhere in the Knight reference is there any indication that these modes are either secure or non-secure. Because the operational modes are not described as being secure or non-secure, Knight certainly cannot disclose both the secure and non-secure modes of the independent claims or the corresponding secure and non-secure exception handlers.

Moreover, even if the Knight reference did disclose secure/non-secure modes, it fails to disclose any "programmable configuration" that controls the mode in which the exception handler is operated. As noted in Knight at paragraph 0019, each of the exceptions has a corresponding processor mode. Knight's paragraph 0020 states "when an exception is generated, the processor automatically changes to the appropriate mode . . . ." This confirms that the

processor always changes **automatically** to the mode appropriate to the exception being processed and so **the user cannot program the mode** in which a particular exception should be handled.

Thus, there cannot be any "respective programmable configurations associated therewith" in the Knight reference.

3. The Dahan reference does not teach "respective programmable configurations associated therewith."

The Dahan reference clearly fails to teach any "respective programmable configurations associated therewith." In the sentence bridging pages 14 and 15 of the outstanding Official Action, the Examiner alleges that Dahan teaches the claimed "respective programmable configurations associated therewith" of independent claims 1 and 24 at column 16, line 1 to column 20, line 35, with the Examiner suggesting that this discloses "normal/non-secure, and secure modes exceptions/interrupts; SSM monitoring interrupts/exceptions."

Notably absent from the Examiner's allegation is any suggestion that Dahan discloses the claimed "respective programmable configurations associated therewith." Should Applicants have missed the Examiner's discussion of where the claimed "respective programmable configurations associated therewith" is disclosed in Dahan, he is respectfully requested to point out the precise column and line number of such teaching.

The Dahan reference discloses a system in which "when an exception occurs, processor 200 jumps to the corresponding exception vector in an interrupt vector table (IVT) from whee it is re-directed to the specific interrupt routine." However, the interrupt vector table is not secure and cannot be trusted (as discussed at column 10, lines 17-22). Thus, in order to allow interrupts

to be handled while in secure mode, a secure interrupt vector table is provided in the Dahan reference (see column 10, lines 31-32). This is accomplished by remapping the interrupt vector table IVT to a secure interrupt vector table SIVT upon entry to the secure mode (column 19, lines 62-64 and steps 1000 and 1002 shown in Figure 10).

The teaching of this portion of Dahan means that if an exception occurs while in the secure mode, then the processor jumps to the corresponding secure exception vector in the secure interrupt vector table (see column 20, lines 6-10 and steps 1010 and 1012 of Figure 10). The original interrupt vector table IVT is only restored upon exiting the secure mode (steps 1021 or 1031 in Figure 10).

Thus, Dahan does not disclose "programmable configurations." Just as in Christie, the only factor that determines whether to use the non-secure interrupt vectors or the secure interrupt vectors is the **current mode of the processor**. If the processor is currently in the non-secure mode, then a vector from the non-secure interrupt vector table is used. If the processor is currently in the secure mode, then a vector from the secure interrupt vector table is used. It is not possible to use a non-secure vector while in secure mode, because the interrupt vector table IVT has been re-mapped to the secure interrupt vector table so that the non-secure vectors are no longer accessible. Similarly, the secure interrupt vector table is not accessible while in the non-secure mode.

Therefore, there is no way possible for the mode for handling an exception to be "programmably configured" and therefore Dahan, like Christie and Knight, fails to teach the claimed "respective programmable configurations associated therewith."

In view of the above understanding of the lack of any support in Christie, Knight or Dahan for the Examiner's fact statements, even if these references are combined as suggested by the Examiner (Christie and Knight or Christie and Dahan), the combination cannot disclose the subject matter of independent claims 1 and 24.

Specifically, the Examiner is reminded that the Court of Appeals for the Federal Circuit has held that "the PTO has the burden under Section 103 to establish a *prima facie* case of obviousness." *In re Fine*, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). "It can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references." There is no disclosure in any of the references of "respective programmable configurations associated therewith."

With respect to the alleged motivation for combining these references, the Examiner has provided no support. In the recent case of *In re Rouffet* , 47 USPQ2d 1453, 1458 (Fed. Cir. 1998), the Court held that "the examiner must show reasons that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed." Nowhere in either of the cited references does there appear to be any recognition of the problem solved by the claimed invention.

The Examiner fails to provide the required explicit "analysis" as to his rationale for picking and choosing elements or interrelationships from the different references and then combining them in the manner disclosed only by Applicants' independent claims 1 and 24. In its recent decision, the U.S. Supreme Court in *KSR International Co. v. Teleflex Inc.*, 82 USPQ2d

1385 (April 2007), held that "[t]o facilitate review [of the Examiner's rationale], this analysis should be made explicit." *Id.* at 1396.

The Supreme Court in its *KSR* decision went on to say that it followed the Court of Appeals for the Federal Circuit's advice that "rejections on obviousness grounds **cannot be sustained by mere conclusory statements**; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness" (emphasis added, the Supreme Court quoting from the Court of Appeals for the Federal Circuit in *In re Kahn*, 78 USPQ2d 1329 (Fed. Cir. 2006)).

The Examiner's sole motivation appears to be that the references are "analogous art because they are from the same field of endeavor." The representation that cited references are from analogous art is not a statement of reasons why one should pick and choose elements and then combine them in the manner of the claims. Because the Examiner has failed to meet his burden of providing an explicit "analysis" as required by the Supreme Court in *KSR*, the Examiner's *prima facie* case of obviousness is not made out, even if the prior art somewhere disclosed the "respective programmable configurations associated therewith" (and, as noted above, this is also missing from all three references).

Having responded to all objections and rejections set forth in the outstanding Official Action, it is submitted that pending claims 1, 2, 4-11, 13-25, 27-34 and 36-47 are in condition for allowance and notice to that effect is respectfully solicited. In the event the Examiner is of the opinion that a brief telephone or personal interview will facilitate allowance of one or more of the above claims, he is respectfully requested to contact Applicants' undersigned representative.

Respectfully submitted,

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